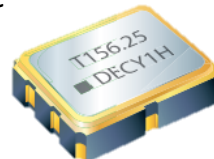


## Product Features

1. 6 pads seam sealed ceramic package
2. Supply Voltage : 1.8 , 2.5 , 3.3V (Typ.)
3. Output Type : LVPECL / LVDS / HCSL
4. Excellent low phase noise and jitter
5. High Power Supply Noise Rejection Performance
6. Tri-state function available
7. RoHS and REACH Compliant , Pb-free , Halogen-free
8. Industry Standard Package :  
2.5 x 2.0 x 0.94 mm

Application :

- Optical Modules
- High Speed Network Interface Cards
- Data Center Switch
- High Performance Computing



● Table 1 . Electrical Specifications

Test condition  
Ambient temperature : 25 ± 5°C  
Relative humidity : 40% ~ 70%

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions & Notes
<b>LVPECL / LVDS / HCSL Common Electrical Characteristics</b>						
Nominal Frequency	F	50 ~ 156.25			MHz	3rd Overtone
Frequency Stability	ST	± 25			ppm	@ -40~85°C , Note 1
		± 50				@ -40~105°C , Note 1
Operating Temperature	Topr	-40	-	85	°C	
		-40	-	105		
Supply Voltage	Vdd	1.8 , 2.5 , 3.3 (± 10%)			V	
Symmetry	TH/T	45	50	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
<b>LVPECL Electrical Characteristics</b>						
Current Consumption	Icc	-	-	40	mA	RL=50Ω to VDD-2V
Standby Current	Icc(ST)	-	-	20	uA	OE = Low
Output Voltage High	VoH	VDD-1.025	-	VDD-0.74	V	
Output Voltage Low	VoL	VDD-1.81	-	VDD-1.405	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2 , (Logic 1)
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2 , (Logic 0)
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.1	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note3

Test condition

 Ambient temperature :  $25 \pm 5^{\circ}\text{C}$ 

Relative humidity : 40% ~ 70%

## ● Table 1 . Electrical Specifications (Continued)

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
<b>LVDS Electrical Characteristics</b>						
Current Consumption	I <sub>cc</sub>	-	-	40	mA	RL=100Ω
Standby Current	I <sub>cc</sub> (ST)	-	-	15	uA	OE = Low
Output Voltage High	V <sub>oH</sub>	-	1.43	1.6	V	
Output Voltage Low	V <sub>oL</sub>	0.9	1.1	-	V	
Offset Voltage	-	1.125	1.250	1.375	V	
Output Swing (Single)	-	247	330	454	mV	Single Peak-to-Peak
Output Swing (Differential)	V <sub>diff</sub>	494	660	908	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.35	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.2	ps	Integrated from 12KHz ~ 20MHz @156.25MHz , 3.3V , Note3
<b>HCSL Electrical Characteristics</b>						
Current Consumption	I <sub>cc</sub>	-	-	30	mA	RL=50Ω
Standby Current	I <sub>cc</sub> (ST)	-	-	10	uA	OE = Low
Output Voltage High	V <sub>oH</sub>	660	740	850	mV	
Output Voltage Low	V <sub>oL</sub>	-150	0	150	mV	
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High	-	0.7VDD	-	-	V	Note 2
Enable Voltage Low	-	-	-	0.3VDD	V	Note 2
Output Enable Delay Time	-	-	-	2	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	-	0.2	ps	Integrated from 12KHz ~ 20MHz @100MHz , 3.3V , Note3

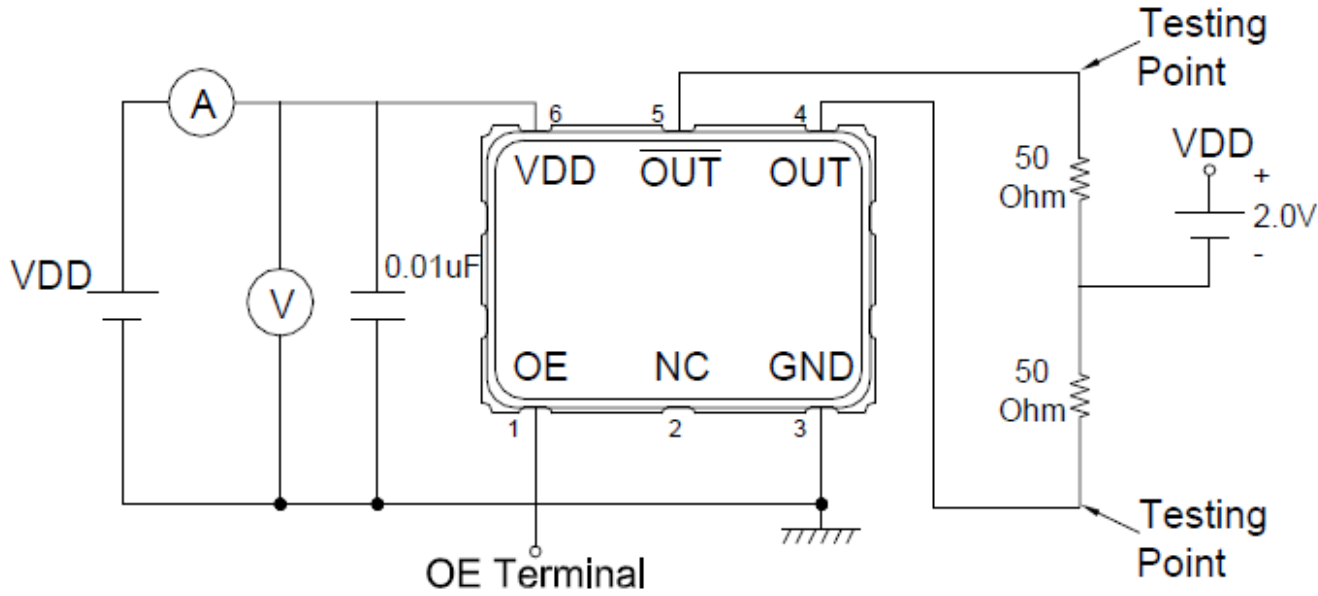
 Note 1 : Inclusive of frequency tolerance at  $25^{\circ}\text{C}$  , variation over temperature , supply voltage variation , 10 years aging and vibration.

Note 2 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.

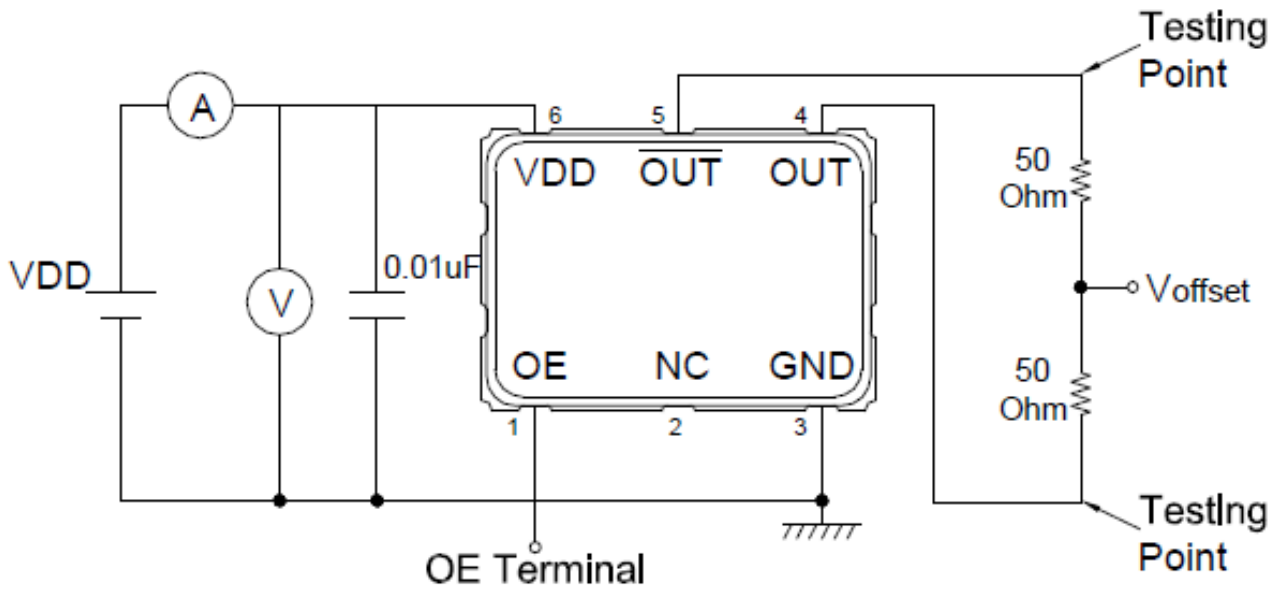
Note 3 : Phase Jitter will be slightly different according to output frequency and supply voltage.

● Test Diagram

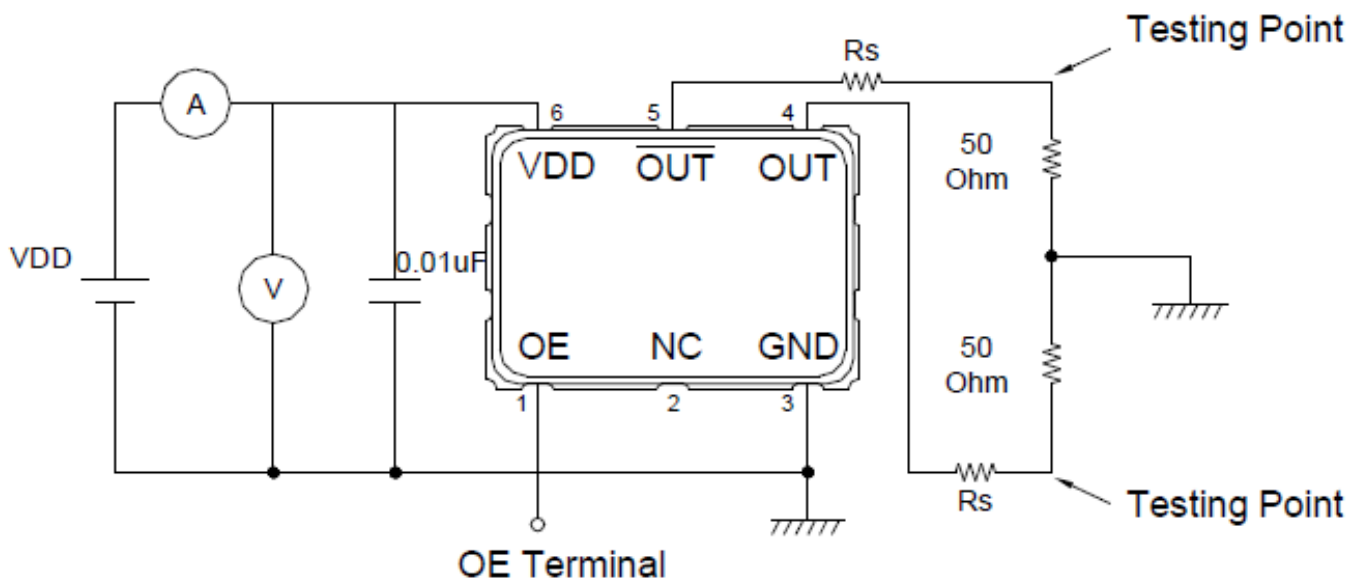
■ LVPECL



■ LVDS



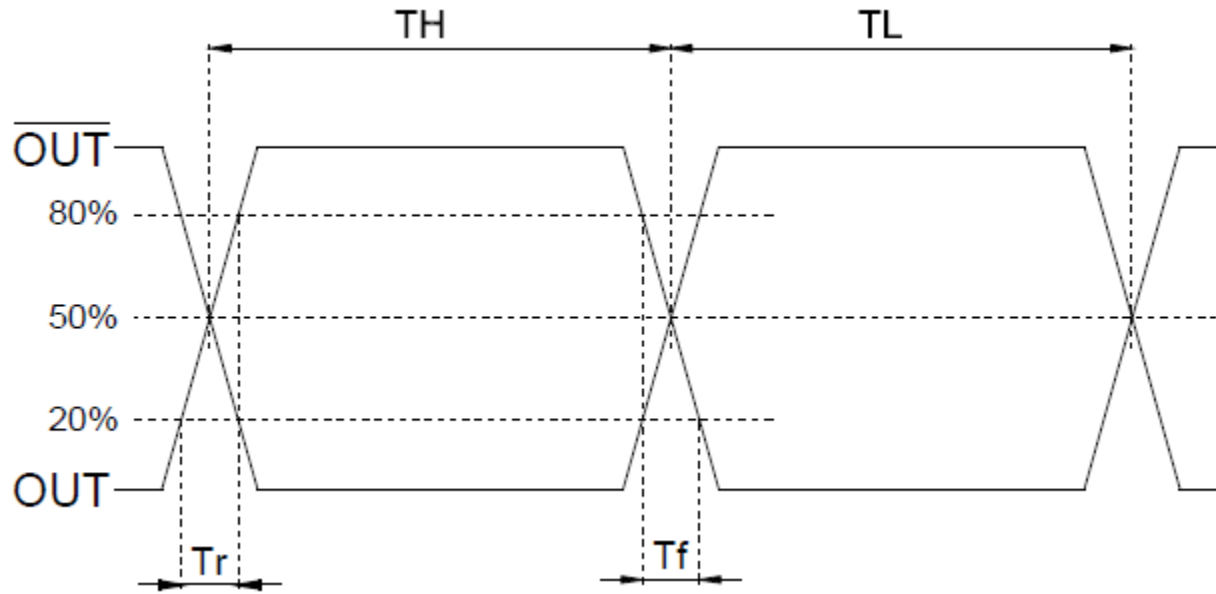
■ HCSL



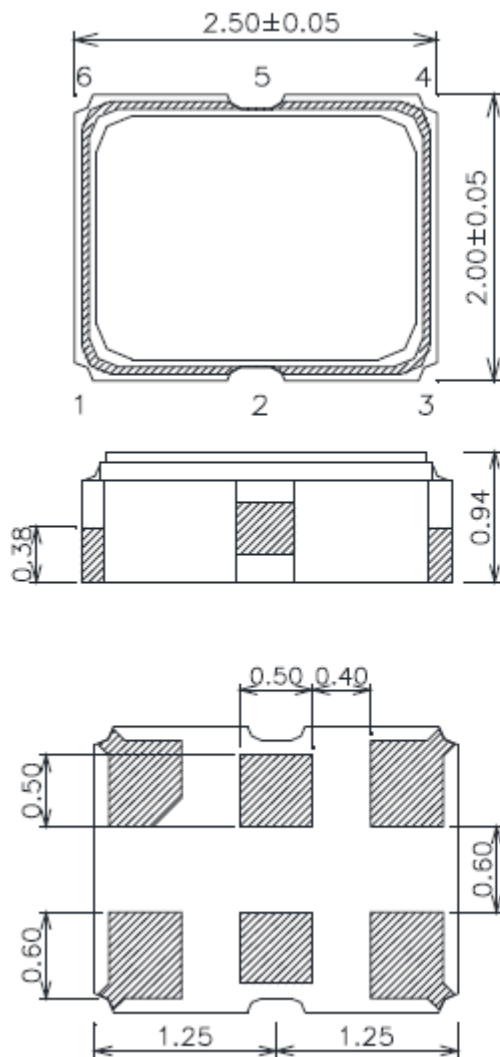
Testing Circuit Note:

1. Above testing circuits cover all the specifications except temperature test & Jitter measurement.
2. All the testing equipment are 50 Ohm terminal.
3. OE terminal is open connection except OE function test.
4. RS= 0 Ohm for test. 0 Ohm to 33 Ohm to minimize overshoot and ring back effect in application.

● **Waveform Conditions**



● **Dimensions & Footprint (Recommended)**

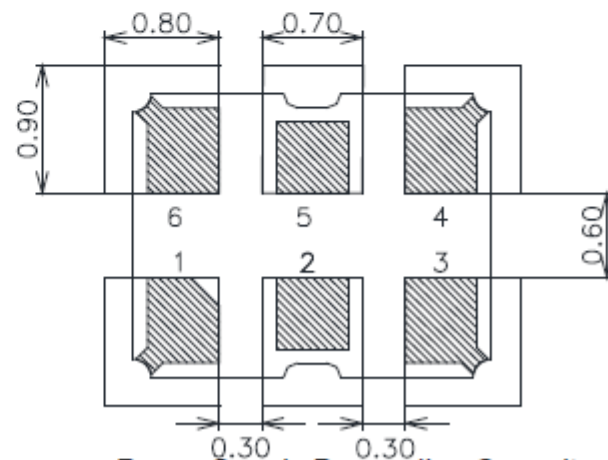


Unit: mm

**Pin Function:**

- 1. OE
- 2. NC
- 3. GND
- 4. OUT
- 5.  $\overline{\text{OUT}}$
- 6. VDD

**Land Pattern:**

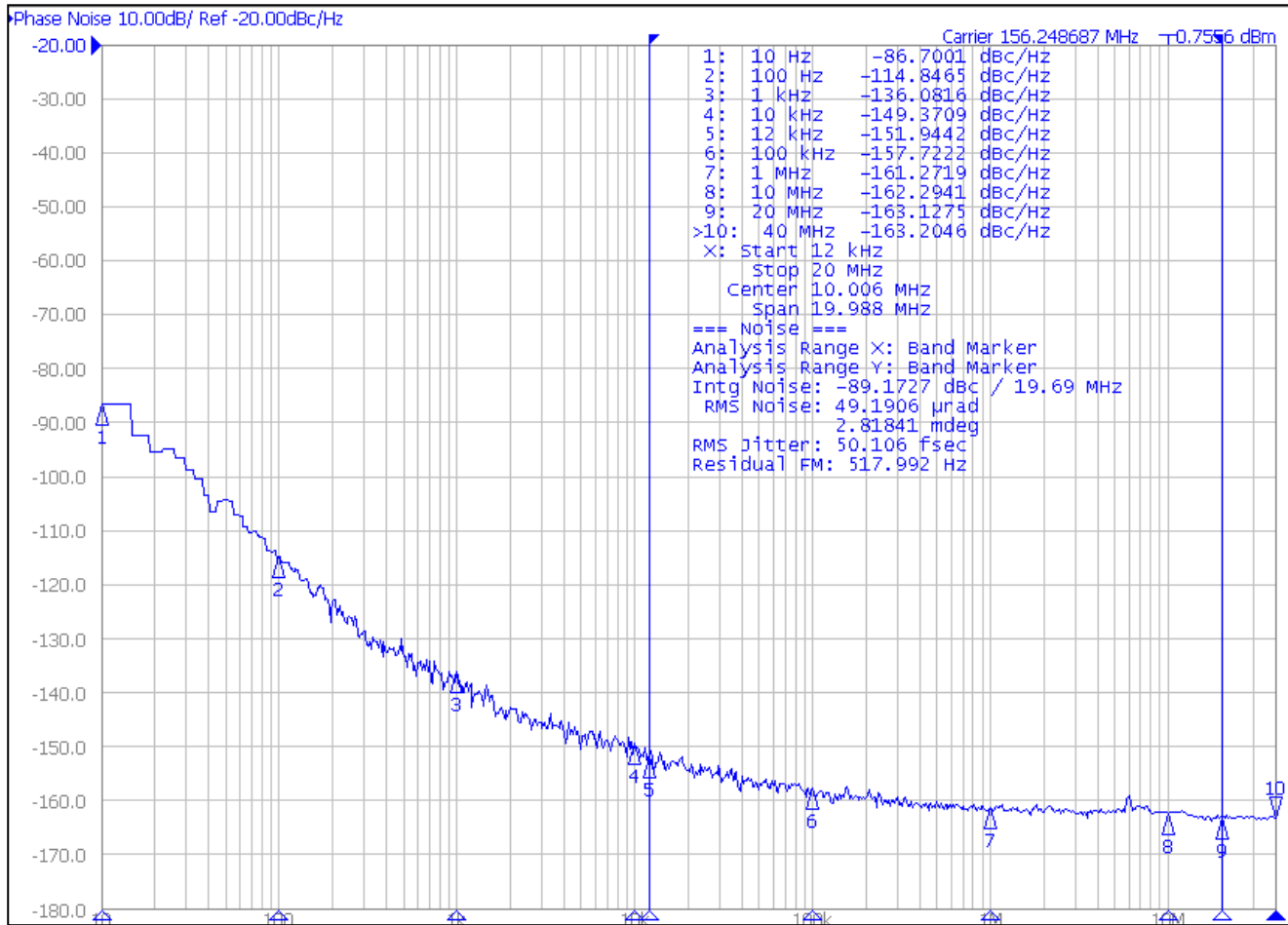


※ Pad dimension tolerance  $\pm 0.2$  mm

※ Power Supply Decoupling Capacitor is Required.

● **Phase Noise & Jitter Performance**

Test Condition : 156.25MHz , 3.3V , LVPECL , @25°C , Integrated from 12KHz ~ 20MHz



● **Power Supply Noise Rejection Performance**

Test Condition : 156.25MHz , 3.3V ( Initial / Add 150m Vp-p White Noise ) , @25°C  
Integrated from 12KHz ~ 20MHz

**Power Supply Noise Rejection**

