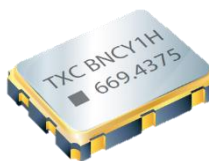


Product Features

1. Output Frequency : 15~2100 MHz
2. Frequency Stability : ± 50 ppm
3. Supply Voltage : 3.3V
4. Operating Temperature : $-40\sim 105^{\circ}\text{C}$
5. Output Type : LVPECL
6. Phase Jitter : 1ps (Max.) @100MHz , 3.3V
7. RoHS and REACH Compliant , Pb-free , Halogen-free
8. Fast Delivery
9. Wide pull range and good linearity.
10. Industry Standard Package :
7.0 x 5.0 x 1.3 mm

Application :

- SDH/ SONET, Ethernet, Base Stations, etc.



Test condition
Ambient temperature : $25 \pm 5^{\circ}\text{C}$
Relative humidity : 40% ~ 70%

Table 1 . Electrical Specifications

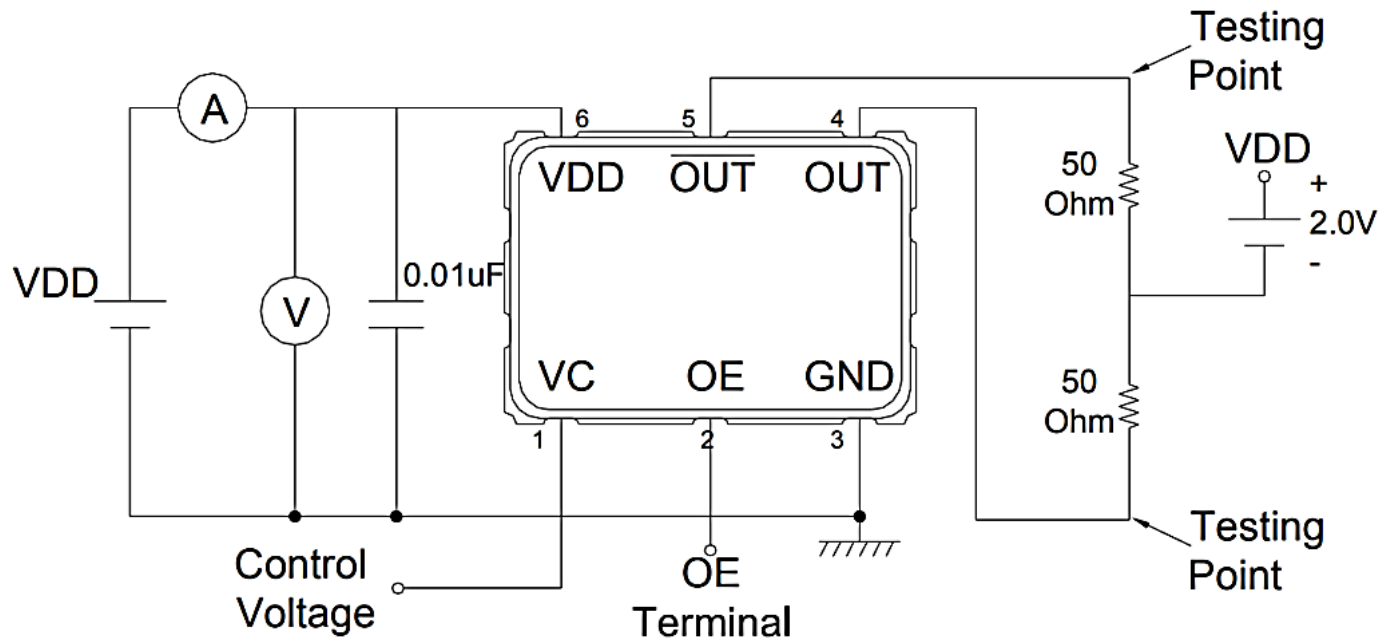
Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
Nominal Frequency	F	15~2100			MHz	
Frequency Tolerance	FT	± 50			ppm	@ $-40\sim 105^{\circ}\text{C}$, Note 1
Operating Temperature	Topr	-40	25	105	$^{\circ}\text{C}$	
Supply Voltage	Vdd	3.3 ($\pm 10\%$)			V	
Nominal center voltage	-	0.5xVdd			V	
Control Voltage Range	Vc	0.1xVdd	-	0.9xVdd	V	
Output Voltage High / Low	VoH/VoL	90%Vdd / 10%Vdd			V	
Symmetry (Duty ratio)	TH/T	45	~	55	%	
Start-up Time	Tosc	-	-	10	ms	To 90% of Final Amplitude
APR	APR	± 50	-	-	ppm	Note2
Linearity	-	-	-	10	%	
Aging	-	± 3			ppm/yr.	1st. Year at 25°C
Current Consumption	Icc	-	93	106	mA	RL=50 Ω to VDD-2V
Standby Current	Icc(ST)	-	91	104	μA	OE = Low
Output Voltage High	VoH	Vdd-1.165	-	Vdd-0.8	V	
Output Voltage Low	VoL	Vdd-2.0	-	Vdd-1.555	V	
Output Voltage Range	Vdiff	600	1400	2000	mV	Differential Peak-to-Peak
Rise / Fall Time	Tr / Tf	-	-	0.5	ns	20% ~ 80% Output Swing
Enable Voltage High / Low	-	0.7xVdd / 0.3xVdd			V	Note 3
Output Enable Delay Time	-	-	-	5	ms	
Output Disable Delay Time	-	-	-	200	ns	
RMS Phase Jitter	PJ	-	0.15~0.2	0.25	ps	Integrated from 12KHz ~ 20MHz @ 156.25MHz , 3.3V

Note 1 : Inclusive of frequency tolerance at 25°C , variation over temperature , supply voltage variation , 10 years aging and vibration.

Note 2 : APR=(Pull Range) - (Frequency tolerance at 25°C , variation over temperature, supply voltage variation, and aging).

Note3 : Output will be enable if OE is Logic 1 or open ; Output will be disable if OE is Logic 0.

● **Test Diagram**

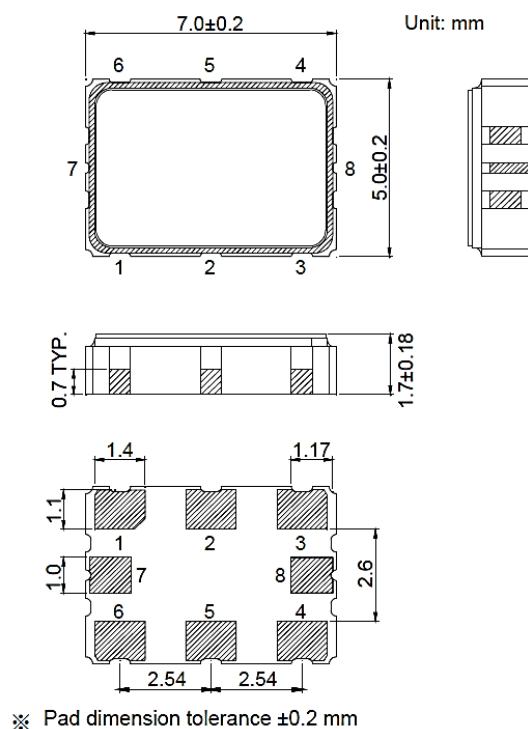


Testing Circuit Note:

1. Above testing circuit covers all the specifications except temperature test & jitter measurement.
2. All the testing equipment are 50Ohm terminal.
3. OE terminal is open connection except OE function test.

● **Dimensions & Footprint (Recommended)**

Unit : mm

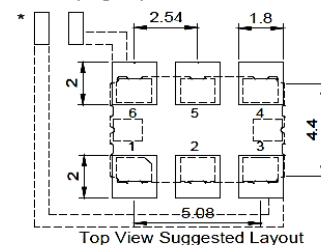


Pin Function:

- | | |
|----------------------------|-------|
| 1. VC | 7. NC |
| 2. OE | 8. NC |
| 3. GND | |
| 4. OUT | |
| 5. $\overline{\text{OUT}}$ | |
| 6. VDD | |

Land Pattern:

* :External high frequency power supply decoupling required.



- ※ Power Supply Decoupling Capacitor is Required.
- ※ Pad dimension tolerance ±0.2 mm